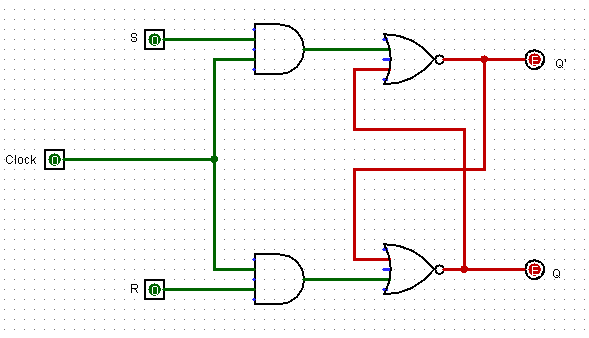
**Title:** CS1026 Lab 5

**Date:** 23/02/2017

**Aim:** To design a gated S-R Flip Flop Circuit that only allows inputs to affect outputs when C=1 and when C=0 it holds the last state value at the output.

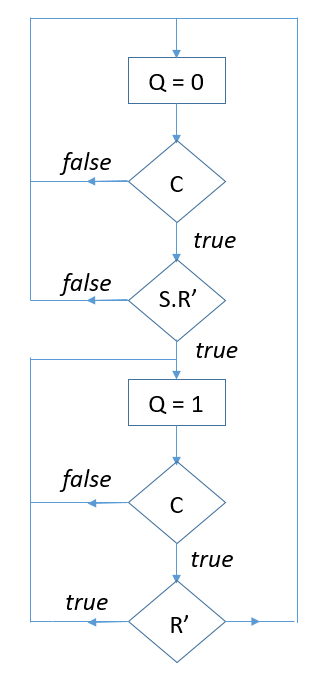
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**Analysis:**

* I began by designing a regular SR Flip-Flop using two NOR gates
* I then added a clock (C) to the circuit and connected it to the S and R inputs using two AND gates
* The results of these AND gates were fed into the two NOR gates that were part of the previous standard SR Flip-Flop
* I then tested the circuit with the various values of S, R and C and observed the outputs Q and Q’ to ensure the clock was serving the desired purpose
* Following this I then designed an ASM for the system (*see next page)*

**Results:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **C** | **S** | **R** | **Q** | **Q’** | **Comment** |
| 1 | 0 | 0 | 0 | 0 | Hold State (null) |
| 1 | 0 | 1 | 0 | 1 | Reset (+clock) |
| 1 | 1 | 0 | 1 | 0 | Set (+clock) |
| 1 | 1 | 1 | 0 | 0 | Illegal State (null) |
| 0 | 0 | 0 | *previous* | *previous* | Holds last |
| 0 | 0 | 1 | *previous* | *previous* | Holds last |
| 0 | 1 | 0 | *previous* | *previous* | Holds last |
| 0 | 1 | 1 | *previous* | *previous* | Holds last |

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